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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,134	12/10/2001	Takashi Yoneda	60188-129	1712

7590 02/09/2005

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EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,134	YONEDA ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4* is/are allowed.

6)☒ Claim(s) *5-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/10/01 & 08/07/0*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is response to the communication filed on 08/07/03 in application 10/006,134.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 5-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants Admitted Prior Art [hereafter referred to as AAPA] (fig. 11-13, Background of the Invention) in view of Hosotani (US Patent 5,701,506).

As per claim 5:

AAPA explicitly teaches:

- A computer device [fig. 11, page 1, line 5] comprising:
- a memory for storing a series of programs [fig. 11, page 1, lines 9-11];
- a CPU for sequentially fetching programs from the memory in a pipeline and decoding and executing the programs [fig. 11, page 1, lines 16-24];
- wherein the CPU fetches a first program from the memory in a fetch cycle [fig. 11, page 1, lines 16-19];

- a decode cycle for the first program [page 1, lines 21-24].

AAPA does not explicitly teach:

- the CPU fetches a second program succeeding to the first program, and also requests the memory to re-read the first program, compares the re-read first program with the first program fetched in the fetch cycle for the first program, and proceeds to execution of the first program if the two programs match with each other.

Hosotani explicitly teaches:

- A microcomputer [abstract, fig. 6, col. 12, lines 12-15]; comprising:

- ***CPU fetching three operation cycles and sequentially outputting program/data for its instruction execution via connectivity among ROM, CPU, matching circuit, comparing circuit, registers, output circuits, etc...*** [fig. 6, col. 5, lines 59 through col. 6, lines 5 and col. 8, lines 9-44].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention was made to apply the ***CPU fetching three operation cycles and***

sequentially outputting program/data for its instruction execution via connectivity among ROM, CPU, matching circuit, comparing circuit, registers, output circuits as taught by Hosotani in conjunction with the computer device having ROM, CPU processing via data, address, and access signals as illustrated by AAPA for performing the detection and correction within the computer device. One of ordinary skill in the art would have been motivated to do so to improve and enhance the computer device operation performance, more specifically to ensuring the data and address stored in memory be analyzed, errors debugged, process diagnostic thoroughly and correctly.
In addition, any error occurred in data memory computing system can be identified, detected, corrected via data matching, comparison, decoding capabilities in providing data/program high reliability, availability, and flexibility environment which eventually will increase its performance throughput.

As per claim 6:

Even thought, AAPA does not explicitly teach:

- if the two programs fail to match with each other, the CPU requests the memory to second re-read the first program, compares the second re-read first program with the

re-read first program, and proceeds to execution of the first program if the two programs match with each other.

Hosotani explicitly teaches:

- A microcomputer [abstract, fig. 6, col. 12, lines 12-15]; comprising:

- ***CPU fetching three operation cycles and sequentially outputting program/data for its instruction execution via connectivity among ROM, CPU, matching circuit, comparing circuit, registers, output circuits, etc***... [fig. 6, col. 5, lines 59 through col. 6, lines 5 and col. 8, lines 9-44].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention was made to apply the ***CPU fetching three operation cycles and sequentially outputting program/data for its instruction execution via connectivity among ROM, CPU, matching circuit, comparing circuit, registers, output circuits*** as taught by Hosotani in conjunction with the computer device having ROM, CPU processing via data, address, and access signals as illustrated by AAPA for performing the detection and correction within the computer device. One of ordinary skill in the art would have been motivated to do so to improve and enhance the computer

device operation performance for the same reasons set forth as described in claim 5, **supra.**

As per claims 7-8:

AAPA explicitly teaches:

- A computer device [fig. 11, page 1, line 5] comprising:

- the memory receives an address signal from the CPU, and outputs a program located at an address corresponding to the address signal and a program at an address immediately preceding the address corresponding to the address signal [fig. 11, page 1, lines 17 through col. 2, line19];

- the memory receives an address signal from the CPU, and outputs a program located at an address corresponding to the address signal and a program at an address immediately preceding the address corresponding to the address signal [fig. 11, page 1, lines 17 through col. 2, line19].

Hosotani further explicitly teaches:

- A microcomputer [abstract, fig. 6, col. 12, lines 12-15]; comprising:

- CPU fetching three operation cycles and sequentially outputting program/data for its instruction execution via connectivity among ROM, CPU, matching circuit, comparing

circuit, registers, output circuits, etc... [fig. 6, col. 5, lines 59 through col. 6, lines 5 and col. 8, lines 9-44].

As per claims 9-10:

AAPA further explicitly teaches:

- a CPU for sequentially fetching programs from the memory in a pipeline and decoding and executing the programs [fig. 11, page 1, lines 16-24];

- a decode cycle for the first program [page 1, lines 21-24].

AAPA does not explicitly teach:

- a latch circuit, wherein the latch circuit latches the first program output from the memory in the fetch cycle in synchronization with the access signal output from the CPU and a match detection circuit for matching programs.

Hosotani explicitly teaches:

- A microcomputer [abstract, fig. 6, col. 12, lines 12-15]; comprising:

- **a *matching circuit, comparing circuit, registers, output circuits, etc***... [fig. 6, col. 5, lines 59 through col. 6, lines 5 and col. 8, lines 9-44].

- ***a synchronization of program outputs and access signal from CPU*** [fig. 11, page 1, lines 9-11];

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention was made to apply the Hosotani's ***matching circuit, comparing circuit, registers, output circuits along with the synchronization of program outputs and access signal from CPU as being the latching and matching circuits*** as claimed by Applicant in conjunction with the computer device having ROM, CPU processing via data, address, and access signals as illustrated by AAPA for performing the detection and correction within the computer device. One of ordinary skill in the art would have been motivated to do so to enhance the computer device operation performance availability and network/system performance throughput therein. In addition, by utilizing these judging circuitries (i.e., comparison, matching, latching, etc...) the computer data and its address stored in memory can be optimized in access location and maximized in performance throughput and process.

9. Claims 1-4 are allowable over the prior art of record.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

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